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DICE Jr / Mini Evaluation Board Hardware Guide

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1 Introduction

The DICE JR/Mini Evaluation board provides an easy to use evaluation and development platform for DICE Jr, DICE Mini and DICE II. By using detachable modules or "Microboards" mounted DICE Jr, DICE Mini or DICE II, engineers can evaluate the performance of the entire DICE family of devices.

The DICE Jr/Mini evaluation board is equipped with the following interfaces: AES3, SPDIF, dual-ADAT, four channels of analog input and output ports for audio, Word-sync, MIDI, two RS232 ports, 8 bit preset, 8 LED's and two data ports for controls. The board can be connected to an IEEE1394 (Firewire) network via two standard 6-pin connectors. The entire board is operated by a DC 9V 1A external power source. The I2S, DSAI and AES3 signals from a DICE family module can be routed to different inputs and/or outputs from the default setup by using audio signal router jumpers placed on the board. Two data ports can be used to connect to external hardware. A DSP module port is also available for additional audio signal processing.

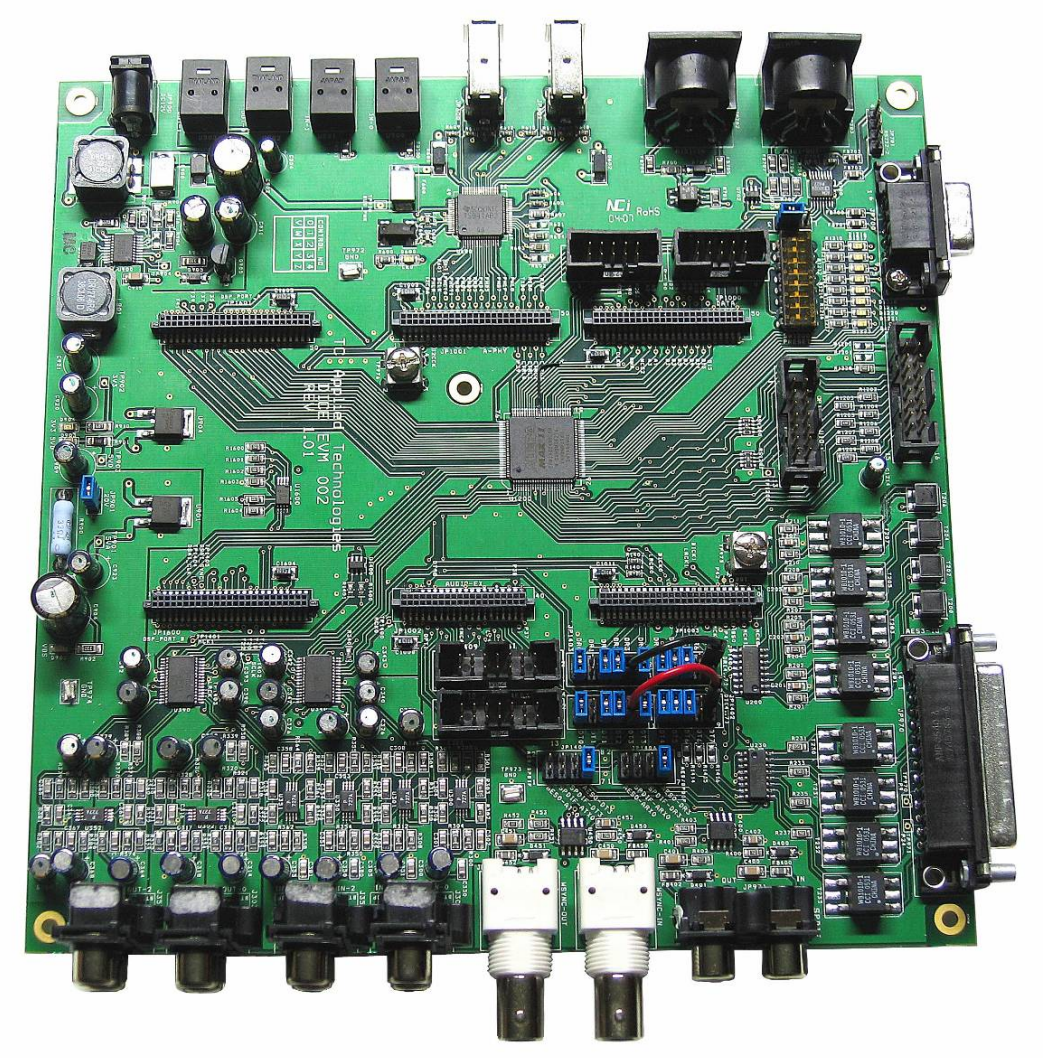


Figure 1: DICE EVM 002 Main Board

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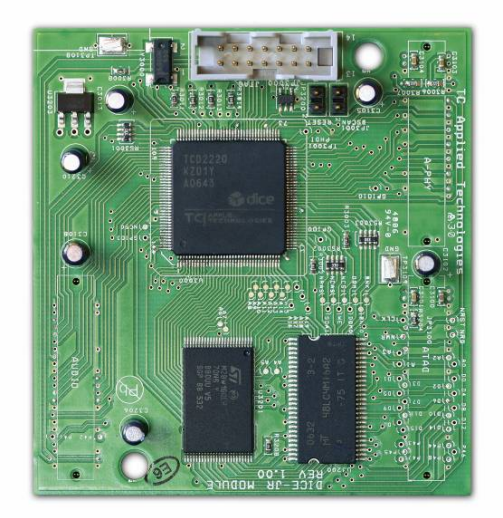


Figure 2: DICE Jr Microboard

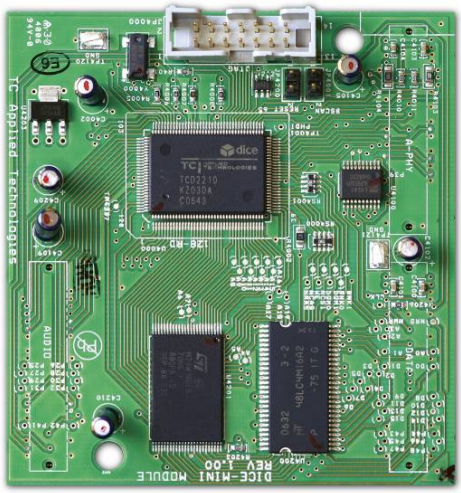


Figure 3: DICE Mini Microboard



Figure 4: DICE II Microboard

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2 DICE™ Jr / Mini Evaluation Board

2.1 Evaluation Board

The DICE Jr/Mini Evaluation board consists of a main board and either a DICE Jr, DICE Mini or DICE II module or "microboard". The DSP module or "microboard", equipped with Motorola DSP56367 and static RAM (512K x 24Bit) is available as an option.

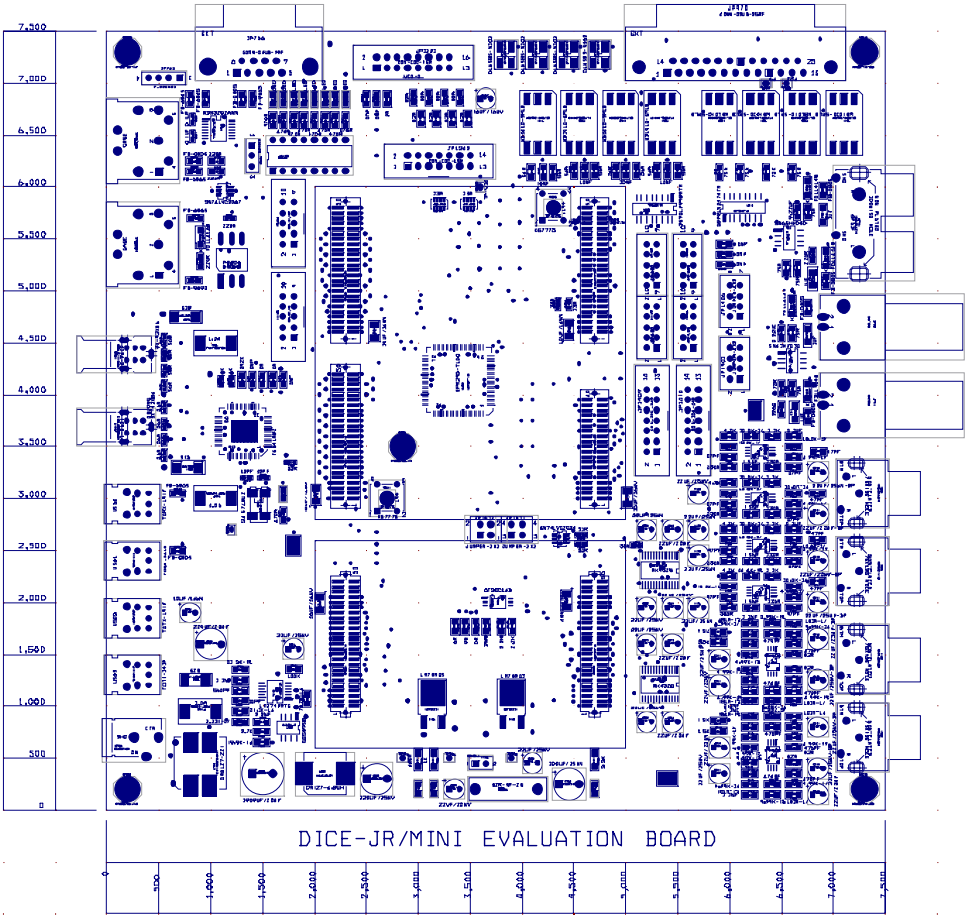


Figure 5: DICE Jr/Mini Evaluation Board

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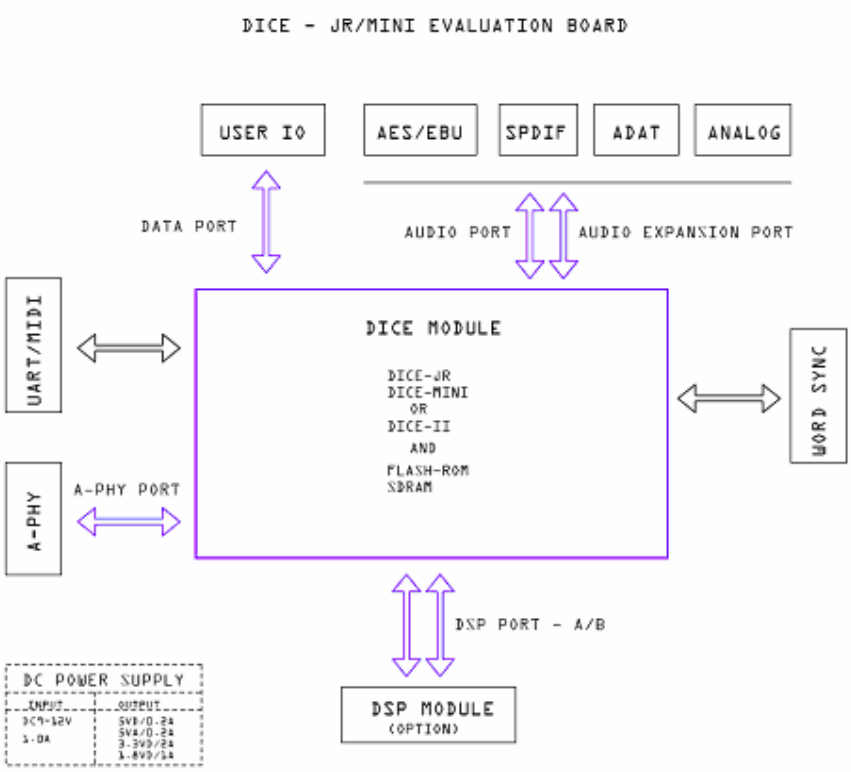


Figure 6: Block diagram

2.2 DC Power requirement

The DICE-Jr/Mini Evaluation board operates with a AC-DC adapter min. 1A, operating range DC 9V to 18V supplied by a centre positive 2.5mm DC plug. A 12V DC supply is recommended.

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3 Inputs, Outputs and User interface

3.1 Audio input and output ports

The evaluation board is designed to enable connection of various end–point audio ports, such as AES, SPDIF, ADAT or analog to available audio ports on a DICE family device using jumper sets. In this sense the jumpers work like a patch-bay.

Connections from the audio ports on DICE-Jr and Mini to the main board are through the DR[0..7] and DT[0..7] ([0..3] for DICE-Mini) transmission lines. These signal lines can be configure to carry various audio signal formats. Please see the User's Guide for further details.

The diagram below shows the relevant audio signals on the DICE 002 EVM, when a DICE Jr or DICE Mini microboard is installed.

The audio signals have some optional routings, which are mainly selected using jumpers.

The DICE II IC, on the other hand, is equipped with dedicated AES and DSAI (TDM) transmission lines. Therefore, the DICE II module is designed to be able to route both groups of signals to DT/DR signal lines using resistor pads.

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3.1.1 AES3 Port

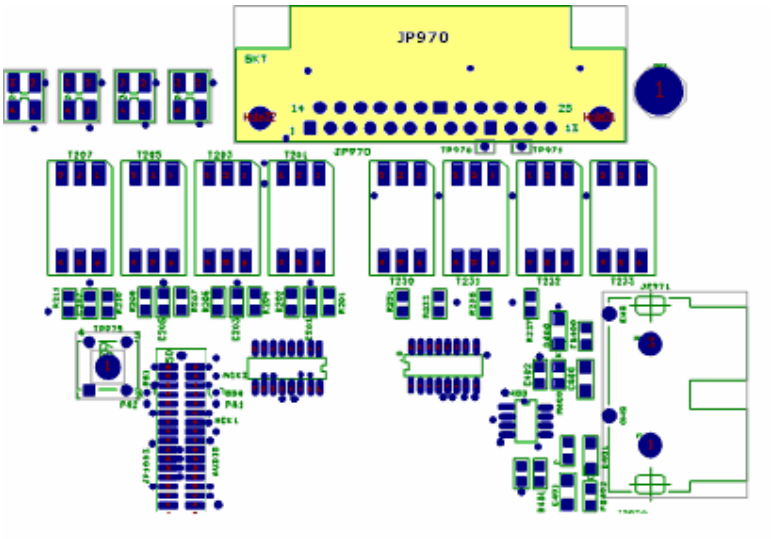


Figure 7: AES3 Input and output port – JP970

PIN	SIGNAL	TYPE
1	CH-0 Input, Pos	I
2	CH-1 Input, Pos	I
3	CH-2 Input, Pos	I
4	CH-3 Input, Pos	I
5	CH-0 Output, Pos	O
6	CH-1 Output, Pos	O
7	CH-2 Output, Pos	O
8	CH3 Output, Pos	O
9	TP970	Tap
10	Shield	
11	Shield	
12	Shield	
13	Shield	
14	CH-0 Input, Neg	I
15	CH-1 Input, Neg	I
16	CH-2 input, Neg	I
17	CH3 input, Neg	I
18	CH-0 Output, Neg	O
19	CH-1 Output, Neg	O
20	CH-2 Output, Neg	O
21	CH-3 Output, Neg	O
22	Shield	
23	Shield	
24	TP971	Tap
25	Shield	

Table 1: AES3-IO DSUB-25RF connector pin assignment

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3.1.2 SPDIF & Word-Sync Port

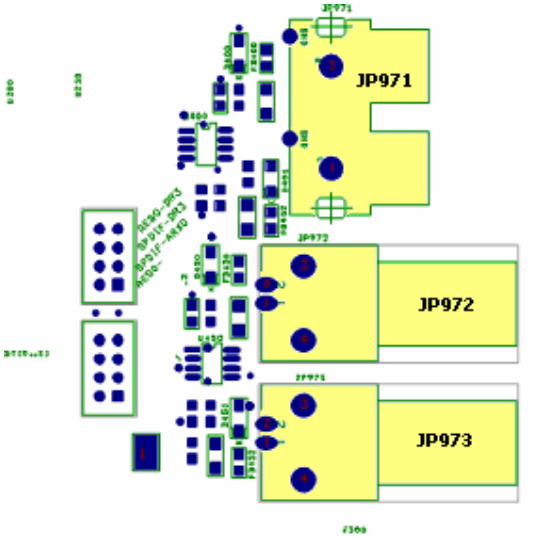


Figure 8: SPDIF – JP971 and Word-sync input JP972 and output JP973 port

3.1.3 ADAT Port

The evaluation board is equipped with two sets of ADAT input and output ports.

On both the DICE Jr and DICE Mini modules, the ADAT-0 port is connected to the DR2/DT2 DICE port. On the DICE-Jr module, the ADAT-1 port is connected to the DR3/DT3 DICE port.

The DICE II module uses only the ADAT-0 port and dedicated OPTI and OPTO transmission lines are therefore used.

On the DICE Jr and Mini modules, the ADAT ports can be configured to carry S/PDIF signals in order to interface with consumer hardware.

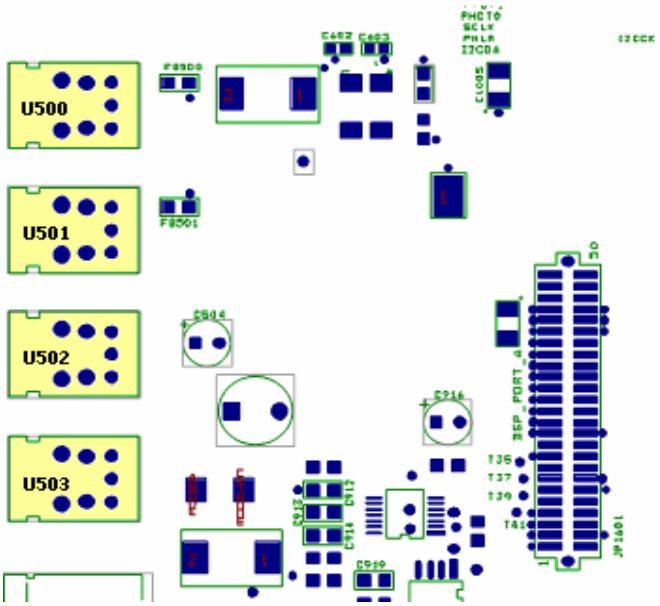


Figure 9: ADAT input U500 and U501and output U502 and U503 port

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3.1.4 Analog Ports

The evaluation board is equipped with four analog input and four analog output channels.

The analog circuit consists of two AKM 24bit/192KHz codec IC's (AK4620A or AK4620B), and six Analog Device dual operational amplifier IC's (OP727).

Internal registers of the AKM codec IC can be accessed from a DICE device using the SPI port in order to change the audio signal format, emphasis, and gain for the DAC. Please refer to AKM's data sheet for further configuration details.

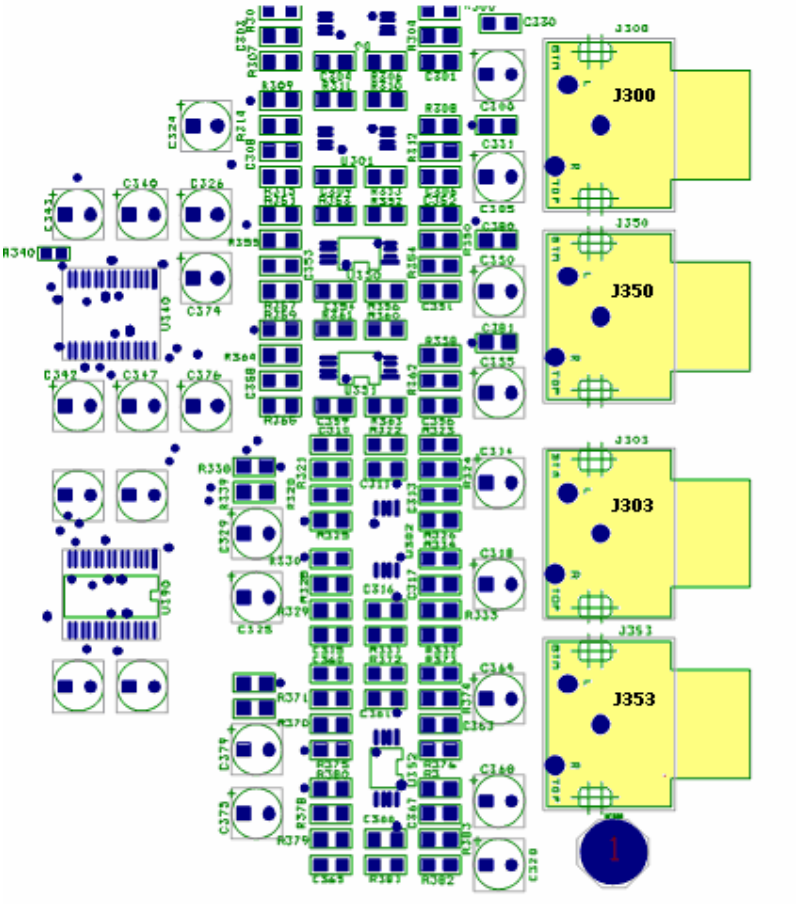


Figure 10: Analog input – J300 and J350 and output J303 and J353 port

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3.2 MIDI and RS232 Port

There are two UART ports on the main board, one with DSUB-9RF connector JP700 and other one with a four pin header JP701.

The second UART port shares signals with the MIDI port. For this reason, when using the second UART port for debugging DICE firmware for instance, make sure to place a jumper on JP704 between pin 1 and 2.

To use the MIDI port, place the jumper between pin 2 and 3 of JP704.

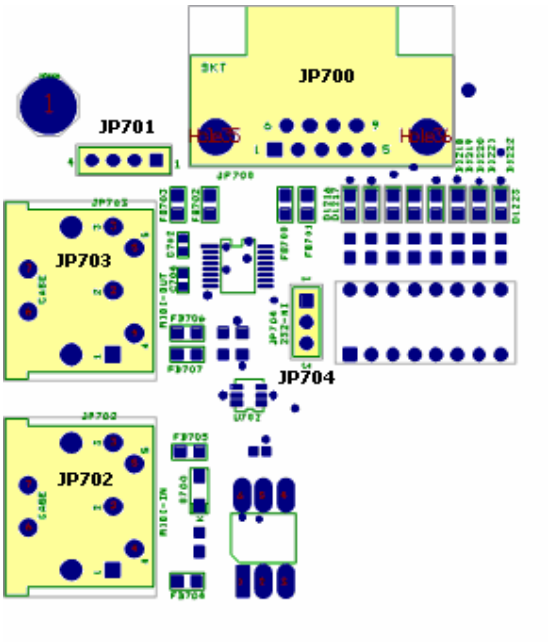


Figure 11: MIDI – JP702 and JP703 and RS232C – JP700 and JP701 port, Serial port 2 function select JP704

PIN	Signal
1	NIL
2	TXD
3	RXD
4	NIL
5	Ground
6	NIL
7	Loop - Connected to Pin 8
8	Loop - Connected to Pin 7
9	NIL

Table 2: RS232C DSUB-9RF connector JP700 pin assignment

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PIN	JP701 Signal
1	Ground
2	TXD
3	Ground
4	RXD

Table 3: RS232C Four pin header JP701 pin assignment

For connecting to a DTE device such as a PC serial port, the cable should connect JP701 TXD pin 2 to RXD on the DTE, RXD pin 4 to TXD, Pin 1 to Ground, and Pin 3 optionally to shield. DICE EVM 002 boards ship with a cable assembly with this configuration.

3.3 IEEE1394 A-PHY Port

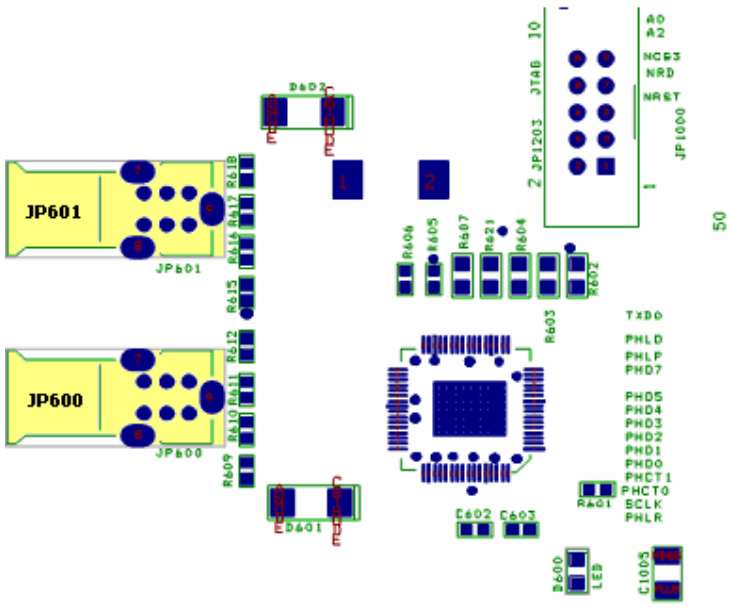


Figure 12: IEEE1394 Firewire ports – JP600 and JP601

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3.4 Data Port, LED and Preset Switch

The LED's, preset switches and data ports are accessible through CPLD U1200's internal byte-wide registers. See section 7 for CPLD configuration.

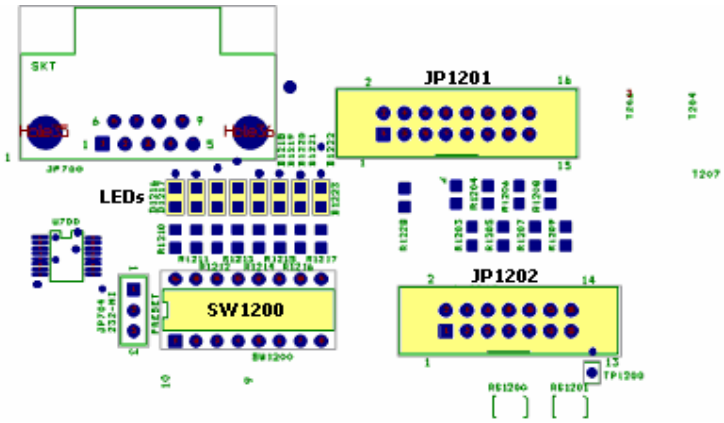


Figure 13: Data port – JP1201 and JP1202, LEDs and preset switch – SW1200

NC2	A[0..2]	BIT	Description	Default value	Access Mode
0	000	7~0	Control register		R/W
0	001	0	Status Register		R
0	010	7~0	UIB_D port data		R/W
0	011	7~0	LED data		R/W
0	100	3~0	DIP Switch data		R
0	101	7~0	Reserved		-
0	110	7~0	Reserved	0	-
0	111	7~0	Firmware version	0x12	R
1	XXX		Invalid		

Table 4: CPLD – U1200 register address map
See table 22 for bit definitions.

In order to be used with firmware, the CPLD must be programmed with revision 1.2 or later. CPLD Contact TCAT for CPLD code and documents relating to CPLD programming and interfacing with firmware.

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3.4.1 Default Switch functions

The Firmware SDK creates the following default switch functions for SW1200:

SW 1 Determines how the streaming configurations (Modes) are selected

On = Mode is selected by the stored setting in flash memory.
Off = Mode is selected by SW2-4.

SW 2-4 Selects a "myMode" streaming mode configuration. See the table below. Modes differ based on the microboard in use. The Mode is active when the board is reset.

SW 5-8 No user function.

SW2	SW3	SW4	Streaming Configuration
Off	Off	Off	Mode0
On	Off	Off	Mode1
Off	On	Off	Mode2
On	On	Off	Mode3
Off	Off	On	Mode4
On	Off	On	Mode5
Off	On	On	Mode6
On	On	On	Mode7

Table 5: myMode selection for SW1200, switches 2-4

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DICE Mini Microboard

Mode	32k-48k	88.2k-96k	176.4k-192k	Access
0	14x14 SPDIF(2), Analog(4), ADAT(8)	10x10 SPDIF(2), Analog(4), ADAT(4)	8x8 SPDIF(2), Analog(4), ADAT(2)	Accessible through SW2-4, CLI and DICE tool.
1	4x4 Analog(4)	4x4 Analog(4)	4x4 Analog(4)	
2	8x8 Analog(4), AES(2), TOS(2)	8x8 Analog(4), AES(2), TOS(2)	8x8 Analog(4), AES(2), TOS(2)	
3	Usermode default as mode 0	Usermode default as mode 0	Usermode default as mode 0	
4	8x8 I2S (for I2S experiments)	8x8 I2S (for I2S experiments)	8x8 I2S (for I2S experiments)	
5	16x16 I8S (for TDM experiments)	16x16 I8S (for TDM experiments)	8x8 I4S (for TDM experiments)	
6	16x16 Single Isoc testmode	16x16 Single Isoc testmode	8x8 Single Isoc testmode	
7	32x32 Dual Isoc testmode	32x32 Dual Isoc testmode	16x16 Dual Isoc testmode	
8	6x6 Analog(4), SPDIF(2)	6x6 Analog(4), SPDIF(2)	6x6 Analog(4), SPDIF(2)	Accessible through CLI and DICE tool.
9	Same as 6	Same as 6	Same as 6	
10	Same as 7	Same as 7	Same as 7	

Table 6: DICE MINI Mode Streaming Configurations

NOTES:

- When using modes with TOS, TOS is on the first Optical I/O
- Mode 6 and 7 are the standard testmodes (16x16 and 32x32) and are equivalent to the Classic EVM mode 9 and 10
- In flash mode (SW1=on) mode 9,10 will mirror mode 6 and 7 for test compatibility

DICE JR Microboard

Mode	32k-48k	88.2k-96k	176.4k-192k	Access
0	28x28 AES(8), Analog(4), ADAT(16)	20x20 AES(8), Analog(4), ADAT(8)	16x16 AES(8), Analog(4), ADAT(4)	Accessible through SW2-4, CLI and DICE tool.
1	4x4 Analog(4)	4x4 Analog(4)	4x4 Analog(4)	
2	8x8 Analog(4), AES(2), TOS(2)	8x8 Analog(4), AES(2), TOS(2)	8x8 Analog(4), AES(2), TOS(2)	
3	Usermode default as mode 0	Usermode default as mode 0	Usermode default as mode 0	
4	16x16 I2S (for I2S experiments)	16x16 I2S (for I2S experiments)	16x16 I2S (for I2S experiments)	
5	32x32 I8S (for TDM experiments)	32x32 I8S (for TDM experiments)	16x16 I4S (for TDM experiments)	
6	16x16 Single Isoc testmode	16x16 Single Isoc testmode	8x8 Single Isoc testmode	
7	32x32 Dual Isoc testmode	32x32 Dual Isoc testmode	16x16 Dual Isoc testmode	
8	6x6 Analog(4), SPDIF(2)	6x6 Analog(4), SPDIF(2)	6x6 Analog(4), SPDIF(2)	Accessible through CLI and DICE tool.
9	Same as 6	Same as 6	Same as 6	
10	Same as 7	Same as 7	Same as 7	

Table 7: DICE JR Mode Streaming Configurations

NOTES:

- When using modes with TOS, TOS is on the first Optical I/O
- Mode 6 and 7 are the standard testmodes (16x16 and 32x32) and are equivalent to the Classic EVM mode 9 and 10
- In flash mode (SW1=on) mode 9,10 will mirror mode 6 and 7 for test compatibility

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DICE II Microboard

Mode	32k-48k	88.2k-96k	176.4k-192k	Access
0	20x20 AES(8), Analog(4), ADAT(8)	16x16 AES(8), Analog(4), ADAT(4)	8x8 AES(4), Analog(4), AES is dual wire.	Accessible through SW2-4, CLI and DICE tool.
1	4x4 Analog(4)	4x4 Analog(4)	4x4 Analog(4)	
2	8x8 Analog(4), AES(4)	8x8 Analog(4), AES(4)	8x8 Analog(4), AES(4)	
3	Usermode	Usermode	Usermode	
4	16x16 I2S (for I2S experiments)	16x16 I2S (for I2S experiments)	12x12 I2S (for I2S experiments)	
5	32x32 I8S (for TDM experiments)	32x32 I8S (for TDM experiments)	16x16 I4S (for TDM experiments)	
6	16x16 Single Isoc testmode	16x16 Single Isoc testmode	8x8 Single Isoc testmode	
7	32x32 Dual Isoc testmode	32x32 Dual Isoc testmode	16x16 Dual Isoc testmode	
8	Same as mode 0	Same as mode 0	Same as mode 0	Accessible through CLI and DICE tool.
9	Same as 6	Same as 6	Same as 6	
10	Same as 7	Same as 7	Same as 7	

Table 8: DICE II Mode Streaming Configurations

3.4.2 Default LED indications

The Firmware SDK creates the following default LED indications:

LED MODE 1	(switch 1 in the OFF position)
LED 1	Toggle when firmware is running (1Hz)
LED 2	Computer is attached and streaming enabled
LED 3	Main clock domain is locked
LED 4	Main AES Master is locked
LED 5	The ADAT Receiver is locked
LED 6	The ADAT Aux Receiver is locked (Mini/JR only)
LED 7	Unused
LED 8	Unused
LED MODE 2	**(switch 1 in the ON position)**
LED 1-4	Meter showing Analog in 1L level
LED 5-8	Meter showing Analog in 1R level

Table 9: LED indications

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Pin	Signal Name
1	Ground
2	VCC, 3.3V or 5V
3	UIA_D0 or Fix DC Voltage
4	UIA_D1
5	UIA_D2
6	UIA_D3
7	UIB_D0
8	UIB_D1
9	UIB_D2
10	UIB_D3
11	UIB_D4
12	UIB_D5
13	UIB_D6
14	UIB_D7
15	Ground
16	3.3V

Table 10: UIO_0 connector JP1201 pin assignment

3.5 Data Extension & CPLD JTAG Port

The user interface CPLD, U1200 is configured so that it can be accessed from the ARM processor on-board the DICE family IC's.

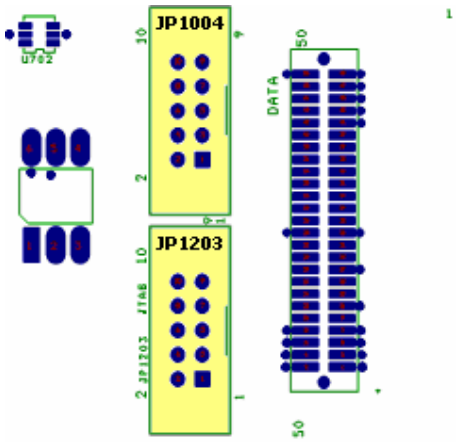


Figure 14: Data port extension – JP1004, and U1200's CPLD JTAG port – JP1203

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Pin	Signal Name
1	3.3V
2	3.3V
3	NCS4
4	NCS5
5	NCS6
6	NCS7
7	A_P47
8	A_P48
9	Ground
10	Ground

Table 11: JP1004 Data expansion port pin assignment

3.6 DICE Module Port

The DICE Jr, DICE Mini and DICE II modules power and signals are connected to the main board through module port connector, JP1000 ~JP1003.

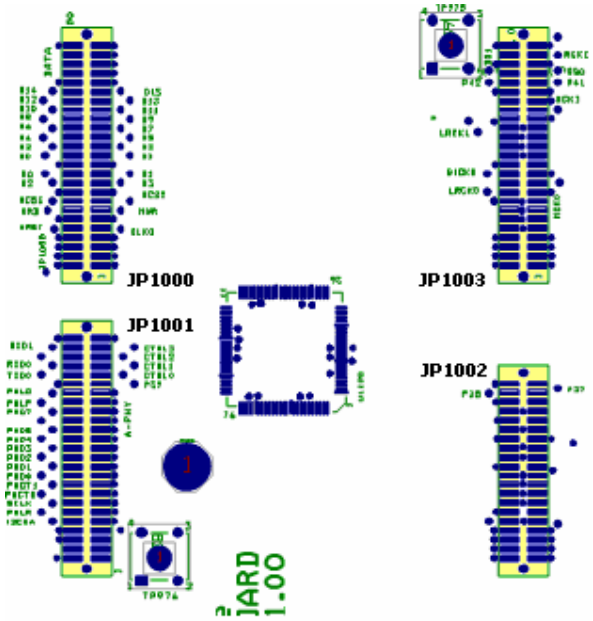


Figure 15: DICE module connector

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3.7 Jumper for voltages exceeding 20V DC

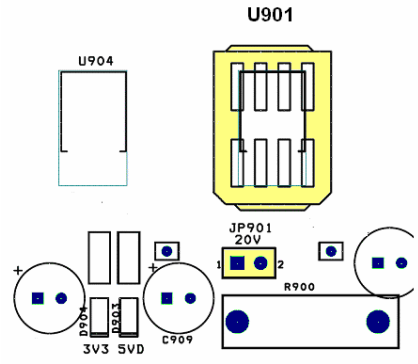


Figure 16: Heat sink on U901, Over 20V jumper JP901

Note:
When heat sink over the U901 is found, do not place shorting jumper on JP901 for all cases.

If the heat sink is not present on U901:

1) When using the supplied external DC power supply, mount the shorting jumper to JP901.

2) When powering the EVM with 1394 bus power from an Apple computer, such as iMac or G5, this shorting jumper must be removed from JP901 to avoid thermal shut-down of DC power supply for analog section of the EVM board.

The EVM002 is equipped with a switched power supply for the digital section of the board. This PSU can handle the wide voltage range for 1394 bus power (12V-30V).

The analog section of the board (Codec and Op-Amps) are powered from a simple linear 5v regulator. It is assumed that customers have their own PSU designs for the analog supplies and for that reason this board contains a very simple analog supply.

This supply does not automatically cope with the huge voltage range available on the 1394 bus. Most PC's providing power will provide 12V which is equivalent to the voltage of the AC adapter supplied with the board.

Some Apple computers supply a much higher voltage, and the linear regulator would go into thermal shut down after a while due to the large voltage drop. To prevent this, the jumper JP901 can be removed which will insert a resistor to handle part of the drop. In this case the 12V supply will not be able to drive the analog section.

The practical result of this is:

- If JP901 is removed the analog inputs and outputs will not work or perform poorly if less than 20V is provided.
- If JP901 is mounted and the supply is higher than 15V the regulator will heat up and might go into thermal shut down in which case the analog inputs and outputs will stop working.

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4 I2S, DSAI, AES3 & ADAT Audio Signal Jumpers

4.1 Audio signal Jumper Set

The DICE JR and DICE-Mini audio ports are configurable and can transport either I2S, I8S (TDM), AES3 or ADAT signals. The audio router jumpers JP1400 ~ 1404, JP1411 and 1412 behave like a signal patch-bay, allowing the user to interchange or switch sources and destinations.

When using a DICE II module, AES3 and DSAI (TDM) signals are provided on dedicated input and output pins of the DICE II device. Signal routing resistors (0R or DNP) mounted on the DICE II module must therefore be used in order to properly route audio signals to and from the module's audio port connectors.

Dedicated DSAI and AES3 signal connectors, JP1409 and JP1410 respectively, are provided mainly for applications using the DICE II module.

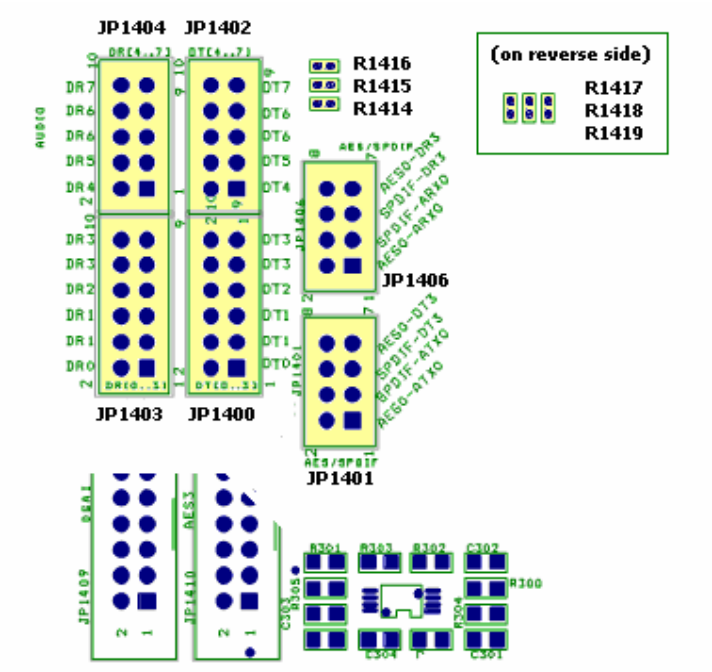


Figure 17: Audio signal routing Jumper Set, Resistor Pads

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4.2 Audio routing – JP1400 ~ JP1404, JP1406

The DICE's I2S, DSAI, AES and ADAT(OPTO) audio signals can be rerouted to and from different source or destination using jumpers, JP1400 to JP1404 and JP1406.

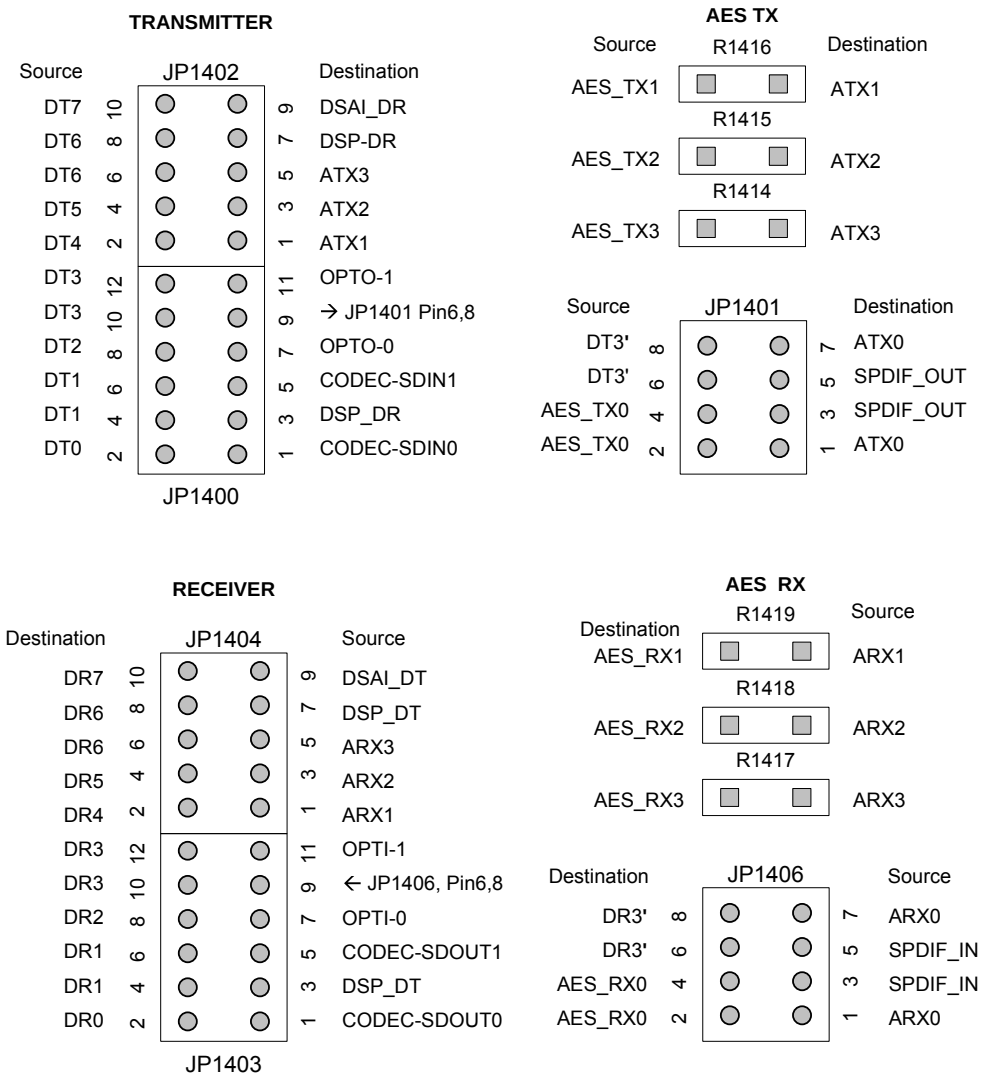


Figure 18: Audio signal routing Jumper Set, Resistor Pads, Signal names

The output source signals, DT0 ~ DT3 on all DICE devices can be routed to CODEC-0, CODEC-1, DSP, ADAT-0,1, AES-0 and SPDIF output using jumpers JP1400 and JP1401. The output source signals, DT4 to DT7 of DICE II and DICE JR can be routed to AES-1 through AES-3 (AES3-IO JP790), DSP-I2S, DSP-DSAI and output using jumper JP1402.

The same applies to all input source signals where the destinations are DR0 ~ DR3 for all DICE devices and DR4 ~ DR7 for DICE II and DICE JR. The Corresponding jumpers for audio signal routing are JP1403, JP1404, and JP1406.

DICE II AES1 ~ AES3 can also be routed to the AES3-IO interface using resistor pads R1414 ~ R1416 (transmit) and R17 ~ R1419 (receive). These are not-placed by default.

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4.2.1 Default Jumper settings for DICE MINI

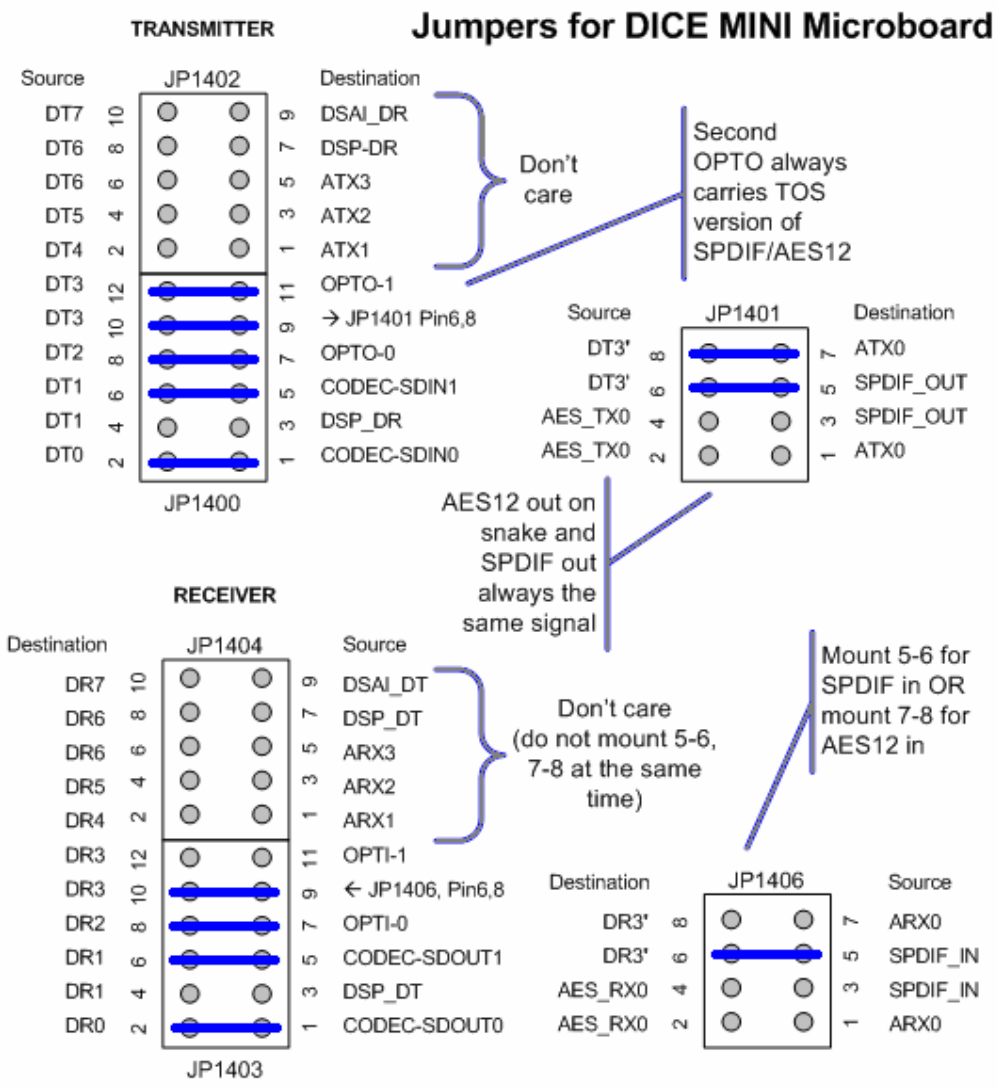


Figure 19: Jumper settings when using the DICE MINI microboard

NOTES:

The AES_TX0_D2 signal is only present on DICE II module (JP1401 1-2, 3-4).

The signal path OPTO_1 to DT3' is only available on DICE JR module.

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4.2.2 Default Jumper settings for DICE JR

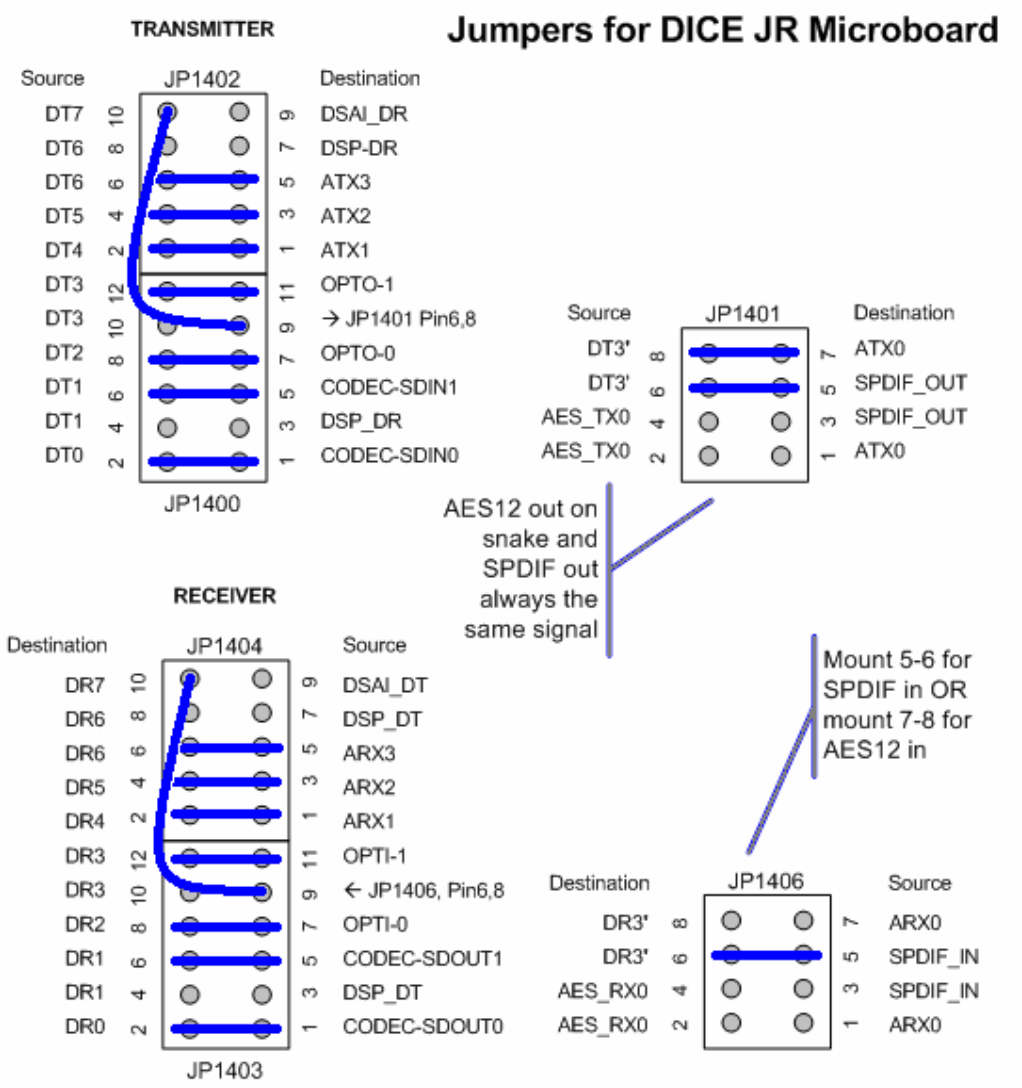


Figure 20: Jumper settings when using the DICE JR microboard

NOTES:

The AES_TX0_D2 signal is only present on DICE II module (JP1401 1-2, 3-4).

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4.2.3 Default Jumper settings for DICE II

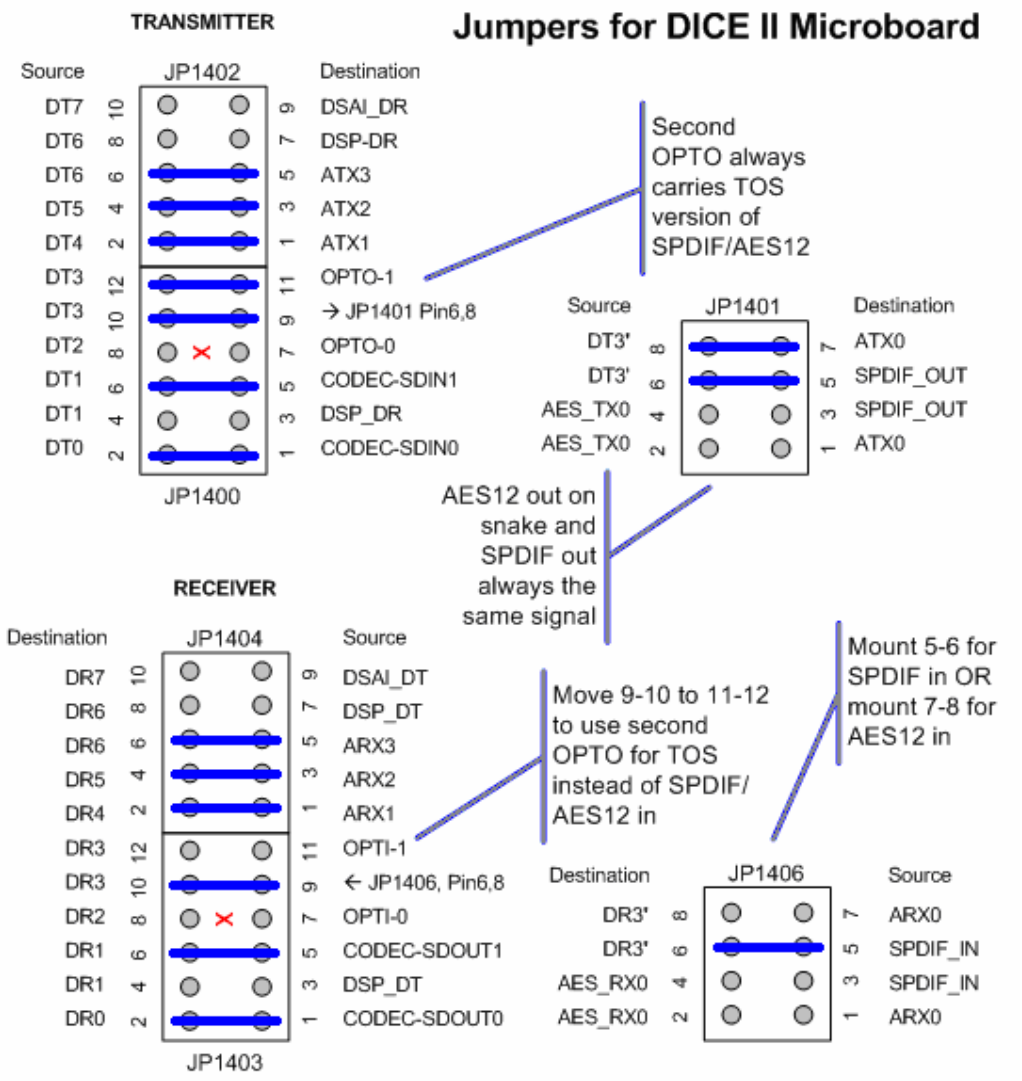


Figure 21: Jumper settings when using the DICE II microboard

NOTES:

The signal path OPTO_1 to DT3' is only available on DICE JR module.

Do not place jumpers across JP1400 7-8 or JP1403 7-8. The DICEII has a dedicated optical port, so it is hardwired. Placing jumpers on those pins would connect them to the I2S0-3 signals, which is not applicable for the DICEII microboard.

The DICEII does not have the pins DT0-7 and DR0-7, rather it has dedicated ports. The microboard is wired to make it as compatible as possible with DICE Jr/Mini.

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4.2.4 DICE Mini Default Jumper Settings

Source	Destination	Jumper(s)
DT0	Codec 0 (Analog Out 1/2)	JP1400 1-2
DT1	Codec 1 (Analog Out 3/4)	JP1400 5-6
DT2	Optical 0 (ADAT-0)	JP1400 7-8
DT3	SPDIF (Ch 1/2)	JP1400 9-10, JP1401 5-6 7-8
DT3	Optical 1 (TOS)	JP1400 11-12

Destination	Source	Jumper(s)
DR0	Codec 0 (Analog In 1/2)	JP1403 1-2
DR1	Codec 1 (Analog In 3/4)	JP1403 5-6
DR2	Optical 0 (ADAT-0)	JP1403 7-8
DR3	SPDIF (Ch 1/2)	JP1403 9-10, JP1406 5-6

Table 12: DICE Mini default Jumper settings

4.2.5 DICE Jr Default Jumper Settings

Source	Destination	Jumper(s)
DT0	Codec 0 (Analog Out 1/2)	JP1400 1-2
DT1	Codec 1 (Analog Out 3/4)	JP1400 5-6
DT2	Optical 0 (ADAT-0)	JP1400 7-8
DT3	Optical 1 (ADAT-1)	JP1400 11-12
DT4	ATX1 (AES Ch 3/4)	JP1402 1-2
DT5	ATX2 (AES Ch 5/6)	JP1402 3-4
DT6	ATX3 (AES Ch 7/8)	JP1402 5-6
DT7	ATX0 (AES Ch 1/2)	JP1402 10 – JP1400 9, JP1401 5-6 7-8

Destination	Source	Jumper(s)
DR0	Codec 0 (Analog In 1/2)	JP1403 1-2
DR1	Codec 1 (Analog In 3/4)	JP1403 5-6
DR2	Optical 0 (ADAT-0)	JP1403 7-8
DR3	Optical 1 (ADAT-1)	JP1403 11-12
DR4	ARX1 (AES Ch 3/4)	JP1404 1-2
DR5	ARX2 (AES Ch 5/6)	JP1404 3-4
DR6	ARX3 (AES Ch 7/8)	JP1404 5-6
DR7	ARX0 (AES Ch 1/2)	JP1403 9 – JP1404 10, JP1406 5-6

Table 13: DICE Jr default Jumper settings

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4.2.6 DICE II Default Jumper Settings

Source	Destination	Jumper(s)
DT0	Codec 0 (Analog Out 1/2)	JP1400 1-2
DT1	Codec 1 (Analog Out 3/4)	JP1400 5-6
DT2	None	Do not place jumper, DICE OPTO hardwired to OPTO-0 (ADAT)
DT3	To JP 1401	JP1400 9-10 and 11-12
DT4	ATX1 (AES Ch 3/4)	JP1402 1-2
DT5	ATX2 (AES Ch 5/6)	JP1402 3-4
DT6	ATX3 (AES Ch 7/8)	JP1402 5-6
DT7	None	

Destination	Source	Jumper(s)
DR0	Codec 0 (Analog In 1/2)	JP1403 1-2
DR1	Codec 1 (Analog In 3/4)	JP1403 5-6
DR2	None	Do not place jumper, DICE OPTI hardwired to OPTI-0 (ADAT)
DR3	TOS OPTI-1 or JP1406	JP1403 9-10 or 11-12 (only mount one)
DR4	ARX1 (AES Ch 3/4)	JP1404 1-2
DR5	ARX2 (AES Ch 5/6)	JP1404 3-4
DR6	ARX3 (AES Ch 7/8)	JP1404 5-6
DR7	None	

Table 14: DICE II default Jumper settings

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5 DICE Modules

Three DICE modules are available, namely the DICE JR, DICE Mini and DICE II modules. All modules are similarly constructed making it easier to switch from one module to the other with minimum setup change on the main board. The main board supplies only 3.3V DC to the module and the necessary 1.8V supplies are internally generated by the module.

The master reset signal NRST and kick-off clock 25MHz signal are also generated by the module. The master system clock SCLK is supplied by the A-PHY device – U600 mounted on the main board.

The JTAG, BSCAN and RESET connectors are provided on the DICE module for testing and firmware development.

5.1 DICE JR Module

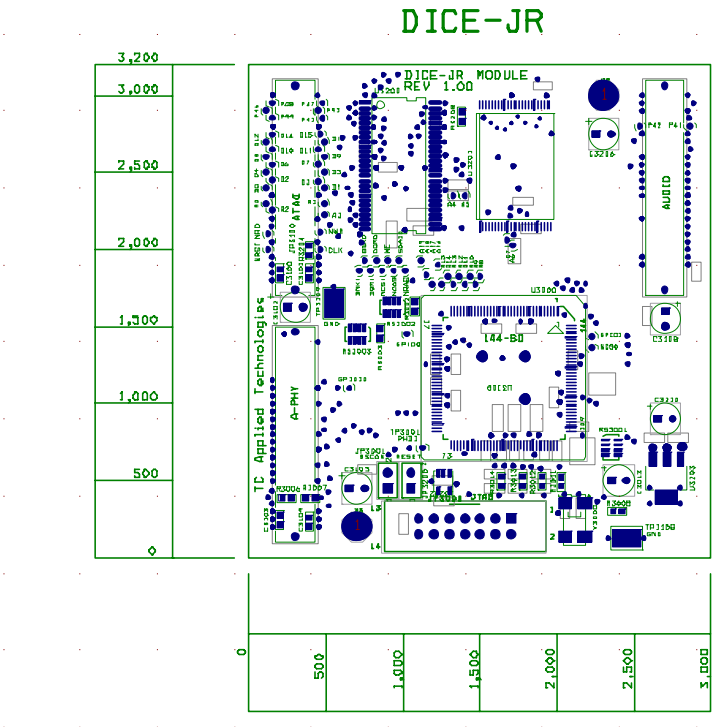


Figure 22: DICE JR module

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Qty	Reference	Part	MFR	MFR PARTS#
1	JP3000	JTAG	3M	2514-6002UB
1	JP3001	BSCAN	WALDOM	22-28-4020
1	JP3100	DATA	AMP	104656-5
1	JP3101	A-PHY	AMP	104656-5
1	JP3102	AUDIO	AMP	104656-5
1	JP3200	RESET	WALDOM	22-28-4020
1	U3000	DICE_JR	TC Applied	TCD2220
1	U3001	LP3990MF-1.8	NS	LP3990MF-1.8
1	U3200	MT48LC4M16A2	MICRON	MT48LC4M16A2-75
1	U3201	AM29LV160B	AMD	AM29LV160EB-70N6
1	U3202	TPS3823-33DBV	TI	TPS3823-33DBVR
1	U3203	LT1963A-1.8	LINEAR	LT1963AEST-1.8
1	Y3000	25.000MHZ	EPSON	MA306 25.0000M-CO

Table 15: DICE JR Module main component list

5.2 DICE Mini Module

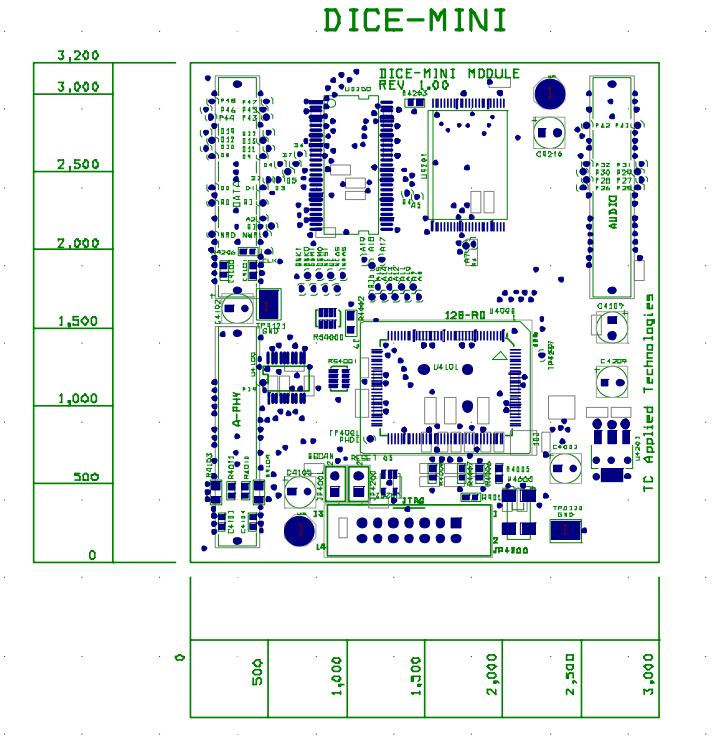


Figure 23: DICE Mini module

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Qty	Reference	Part	MFR	MFR PARTS#
1	JP4000	JTAG	3M	2514-6002UB
1	JP4001	BSCAN	WALDOM	22-28-4020
1	JP4100	DATA	AMP	104656-5
1	JP4101	A-PHY	AMP	104656-5
1	JP4102	AUDIO	AMP	104656-5
1	JP4200	RESET	WALDOM	22-28-4020
1	U4000	DICE_MINI	TC Applied Tech.	TCD2210
1	U4001	LP3990MF-1.8	NS	LP3990MF-1.8
1	U4100	SN74AHC241	TI	SN74AHC241
1	U4200	MT48LC4M16A2	MICRON	MT48LC4M16A2-75
1	U4201	AM29LV160B	AMD	AM29LV160EB-70N6
1	U4202	TPS3823-33DBV	TI	TPS3823-33DBVR
1	U4203	LT1963A-1.8	LINEAR	LT1963AEST-1.8
1	Y4000	25.000MHZ	EPSON	MA306 25.0000M-CO

Table 16: DICE Mini Module main component list

5.3 DICE II Module

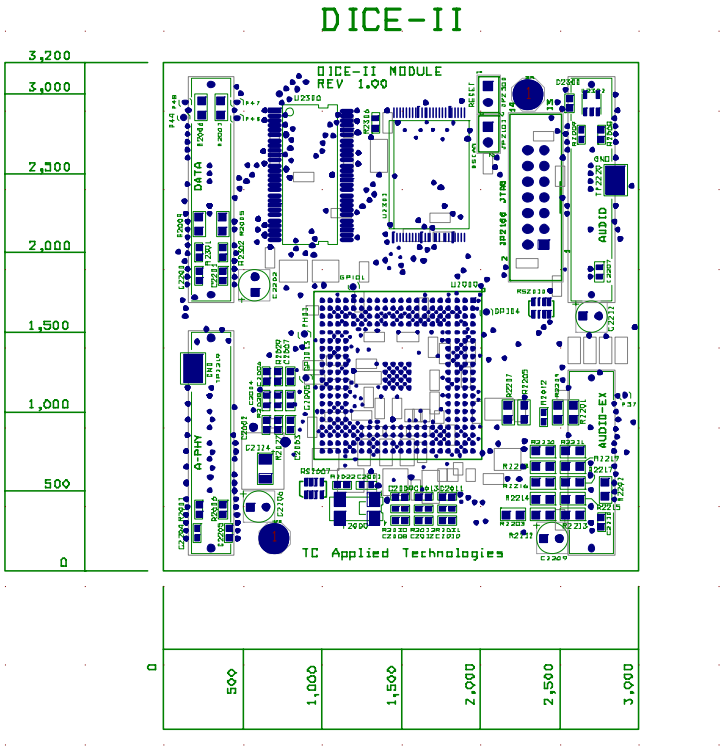


Figure 24: DICE II module

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Qty	Reference	Part	PCB Footprint	MFR
1	JP2100	JTAG	CON-IDC-14M	3M
1	JP2101	BSCAN	CON100-2	WALDOM
1	JP2200	DATA	CONN-SFM-50	AMP
1	JP2201	A-PHY	CONN-SFM-50	AMP
1	JP2202	AUDIO-EX	CONN-SFM-40	AMP
1	JP2203	AUDIO	CONN-SFM-50	AMP
1	JP2300	RESET	CON100-2	WALDOM
1	U2000	DICEII-STD-PBGA272	IC-PBGA-272	
1	U2100	LT1963A-1.8	IC-SOT-223-1234	LINEAR
1	U2101	LP3990MF-1.8	IC-SOT-23-5	NS
1	U2300	MT48LC4M16A2	IC-TSOP-54	MICRON
1	U2301	AM29LV160B	IC-TSOP-48	AMD
1	U2302	TPS3823-33DBV	IC-SOT23-5	TI
1	Y2000	25.000MHZ	XTAL-MA306	EPSON

Table 17: DICE II Module main component list

5.4 DICE Module Dimensions

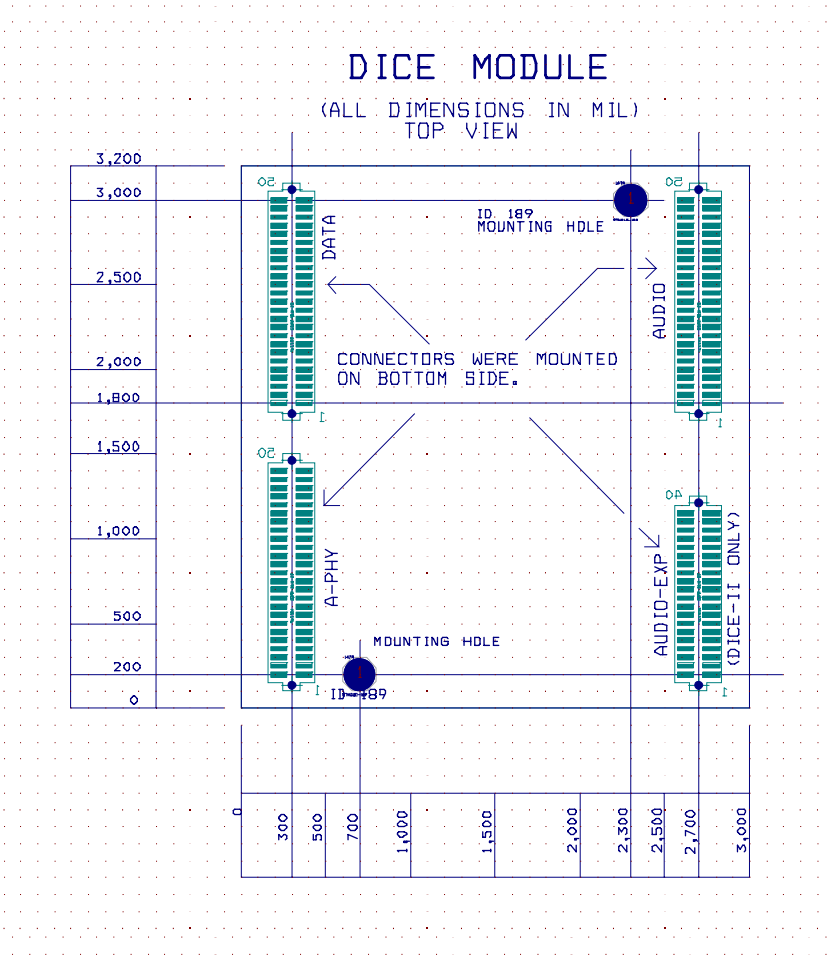


Figure 25: DICE module dimensions

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5.5 Module Connector Pin Signal Assignment

The DICE JR, DICE Mini and DICE II modules are equipped with three connectors, one for each of the Data, A-PHY and Audio ports. In addition, the DICE II module is equipped with an Audio Expansion port connector.

Necessary 3.3V DC power is supplied to the module from the main board through all of these connectors. The two required 1.8V DC supplies for a DICE module are created by the LDO type regulator ICs on the module. The DICE 25MHz system clock CLKO and master reset signal NRST are generated by the module and fed to the main board.

5.5.1 Data port – JP1000

Pin	Signal name	Type	Description	II	JR	MINI
1	3.3V		DC Power			
2	3.3V		DC Power			
3	3.3V		DC Power			
4	3.3V		DC Power			
5	Ground		Ground			
6	Ground		Ground			
7	Ground		Ground			
8	Ground		Ground			
9	CLKO	O	System Clock	√	√	√
10	NRST	O	System Reset. Active low	√	√	√
11	Ground		Ground			
12	Ground		Ground			
13	NWR	O	System Write. Active low	√	√	√
14	NRD	O	System Read. Active low	√	√	√
15	NCS2	O	System Select. Active low	√	√	√
16	NCS3	O		√	√	√
17	Ground		Ground			
18	Ground		Ground			
19	A3	O	Address bit 3	√	√	√
20	A2	O	Address bit 2	√	√	√
21	A1	O	Address bit 1	√	√	√
22	A0	O	Address bit 0	√	√	√
23	Ground		Ground			
24	Ground		Ground			
25	D1	I/O	Data bit 1	√	√	√
26	D0	I/O	Data bit 0	√	√	√
27	D3	I/O	Data bit 3	√	√	√
28	D2	I/O	Data bit 2	√	√	√
29	D5	I/O	Data bit 5	√	√	√
30	D4	I/O	Data bit 4	√	√	√

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31	D7	I/O	Data bit 7	√	√	√
32	D6	I/O	Data bit 6	√	√	√
33	D9	I/O	Data bit 9	√	√	√
34	D8	I/O	Data bit 8	√	√	√
35	D11	I/O	Data bit 11	√	√	√
36	D10	I/O	Data bit 10	√	√	√
37	D13	I/O	Data bit 13	√	√	√
38	D12	I/O	Data bit 12	√	√	√
39	D15	I/O	Data bit 15	√	√	√
40	D14	I/O	Data bit 14	√	√	√
41	Ground		Ground			
42	Ground		Ground			
43	NCS4	I/O	Chip select / GPIO	√		
44	NCS5	I/O	Chip select / GPIO	√		
45	NCS6	I/O	Chip select / GPIO	√		
46	NCS7	I/O	Chip select / GPIO	√		
47	Tap - A_P47		Tap			
48	Tap - A_P48		Tap			
49	Ground		Ground			
50	Ground		Ground			

Table 18: Data port - JP1000

5.5.2 IEEE1394 A-PHY port – JP1001

Pin	Signal name	Type	Description	II	JR	MINI
1	3.3V		DC Power			
2	3.3V		DC Power			
3	3.3V		DC Power			
4	3.3V		DC Power			
5	Ground		Ground			
6	Ground		Ground			
7	I2CCK	I/O	I2C Clock	√	√	√
8	Ground		Ground			
9	Ground		Ground			
10	I2CDA	I/O	I2C Data	√	√	√
11	PHLR	O	PHY Lock Request	√	√	√
12	Ground		Ground			
13	Ground		Ground			
14	SCLK	O	PHY Clock	√	√	√
15	PHCT0	I/O	PHY Control bit 0	√	√	√
16	Ground		Ground			
17	Ground		Ground			
18	PHCT1	I/O	PHY Control bit 1	√	√	√

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19	PHD0	I/O	PHY Data bit 0	√	√	√
20	Ground		Ground			
21	Ground		Ground			
22	PHD1	I/O	PHY Data bit 1	√	√	√
23	PHD2	I/O	PHY Data bit 2	√	√	√
24	Ground		Ground			
25	Ground		Ground			
26	PHD3	I/O	PHY Data bit 3	√	√	√
27	PHD4	I/O	PHY Data bit 4	√	√	√
28	Ground		Ground			
29	Ground		Ground			
30	PHD5	I/O	PHY Data bit 5	√	√	√
31	PHD6	I/O	PHY Data bit 6	√	√	√
32	Ground		Ground			
33	Ground		Ground			
34	PHD7	I/O	PHY Data bit 7	√	√	√
35	PHLP	O		√	√	√
36	Ground		Ground			
37	Ground		Ground			
38	PHLO	I	PHY Locked	√	√	√
39	Tap - P39					
40	Ground		Ground			
41	CTRL0	I/O	SPI Control bit 0	√	√	√
42	TXD0	O	UART TX-0	√	√	√
43	CTRL1	I/O	SPI Control bit 1	√	√	√
44	RXD0	I	UART RX-0	√	√	√
45	CTRL2	I/O	SPI Control bit 2	√	√	√
46	TXD1	O	UART TX-1	√	√	√
47	CTRL3	I/O	SPI Control bit 3	√	√	√
48	RXD1	I	UART RX-1	√	√	√
49	Ground		Ground			
50	Ground		Ground			

Table 19: IEEEE1394 A-PHY port - JP1001

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5.5.3 Audio port – JP1003

Pin	Signal name	Type	Description	II	JR	MINI
1	3.3V		DC Power			
2	3.3V		DC Power			
3	3.3V		DC Power			
4	3.3V		DC Power			
5	Ground		Ground			
6	Ground		Ground			
7	Ground		Ground			
8	Ground		Ground			
9	DR0	I	I2S Receive - 0	√	√	√
10	DT0	O	I2S Send - 0	√	√	√
11	DR1	I	I2S Receive - 1	√	√	√
12	DT1	O	I2S Send - 1	√	√	√
13	DR2	I	I2S Receive - 2	√	√	√
14	DT2	O	I2S Send - 2	√	√	√
15	DR3	I	I2S Receive - 3	√	√	√
16	DT3	O	I2S Send -3	√	√	√
17	Ground		Ground			
18	Ground		Ground			
19	MCK0	O	I2S Master clock 0	√	√	√
20	LRCK0	O	I2S Frame clock 0	√	√	√
21	Ground		Ground			
22	BICK0	O	I2S Bit clock 0	√	√	√
23	Ground		Ground			
24	Ground		Ground			
25	DR4	I	I2S Receive - 4	√	√	
26	DT4	O	I2S Send - 4	√	√	
27	DR5	I	I2S Receive - 5	√	√	
28	DT5	O	I2S Send - 5	√	√	
29	DR6	I	I2S Receive - 6	√	√	
30	DT6	O	I2S Send - 6	√	√	
31	DR7	I	I2S Receive - 7	√	√	
32	DT7	O	I2S Send - 7	√	√	
33	Ground		Ground			
34	Ground		Ground			
35	MCK1	O	I2S Master clock 1	√	√	√
36	LRCK1	O	I2S Frame clock 1	√	√	√
37	Ground		Ground			
38	BICK1	O	I2S Bit clock 1	√	√	√

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39	Ground		Ground			
40	Ground		Ground			
41	Tap - P41					
42	Tap - P42					
43	BS0	O	Byte Select - Low	√	√	√
44	BS1	O	Byte Select - High	√	√	√
45	Ground		Ground			
46	Ground		Ground			
47	WCKI	I	Word sync	√	√	√
48	WCKO	O	Word sync	√	√	√
49	Ground		Ground			
50	Ground		Ground			

Table 20: Audio port - JP1003

√ : Refer to DICE module

5.5.4 Audio Extension port – JP1002 (DICE II only)

Pin	Signal name	Type	Description
1	3.3V		DC Power
2	3.3V		DC Power
3	3.3V		DC Power
4	3.3V		DC Power
5	Ground		Ground
6	Ground		Ground
7	Ground		Ground
8	Ground		Ground
9	OPTI	I	ADAT In
10	OPTO	O	ADAT out
11	Ground		Ground
12	Ground		Ground
13	AES_RX0	I	AES3 Receive 0
14	AES_TX0	O	AES3 Send 0
15	AES_RX1	I	AES3 Receive 1
16	AES_TX1	O	AES3 Send 1
17	AES_RX2	I	AES3 Receive 2
18	AES_TX2	O	AES3 Send 2
19	AES_RX3	I	AES3 Receive 3
20	AES_TX3	O	AES3 Send 3
21	Ground		Ground
22	Ground		Ground
23	SYNCA	O	DSAI Sync A
24	SYNCB	O	DSAI Sync B

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25	CKA	O	DSAI Clock A
26	CKB	O	DSAI Clock B
27	Ground		Ground
28	Ground		Ground
29	DSAI_RX0	I	DSAI Receive 0
30	DSAI_TX0	O	DSAI Send 0
31	DSAI_RX1	I	DSAI Receive 1
32	DSAI_TX1	O	DSAI Send 1
33	DSAI_RX2	I	DSAI Receive 2
34	DSAI_TX2	O	DSAI Send 2
35	DSAI_RX3	I	DSAI Receive 3
36	DSAI_TX3	O	DSAI Send 3
37	Tap - P37		
38	Tap - P38		
39	Ground		Ground
40	Ground		Ground

Table 21: Audio extension port - JP1002

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5.5.5 Connector Pin Number

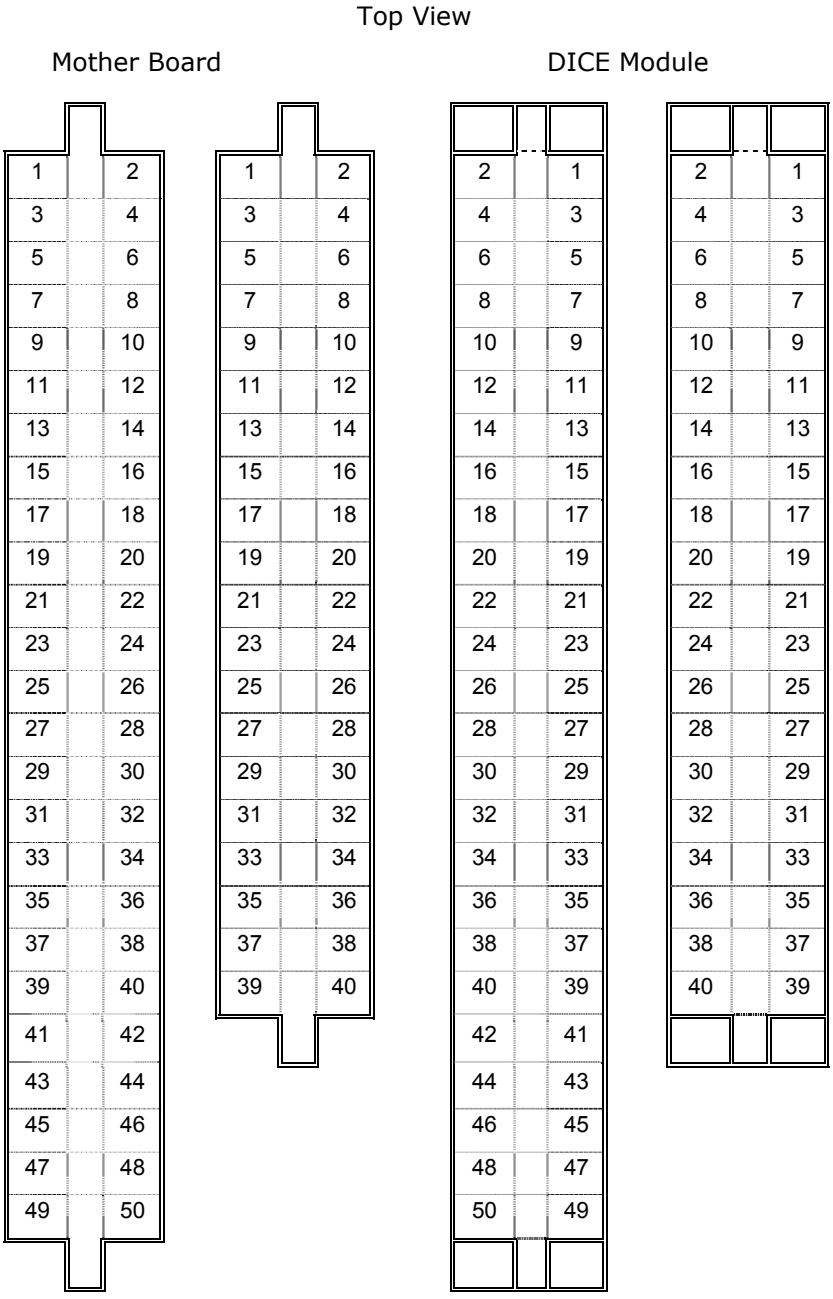


Figure 26: DICE module connector pin-out

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50 position connector		
Manufacturer	**Mother Board**	**DICE Module**
SAMTEC	SFM-125-02-S-D-LC	TFM-125-12-S-D-LC
40 position connector		
Manufacturer	**Mother Board**	**DICE Module**
SAMTEC	SFM-120-02-S-D-LC	TFM-120-12-S-D-LC

Table 22: DICE Module Connector Types

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6 DSP Module Port

6.1 DSP Port

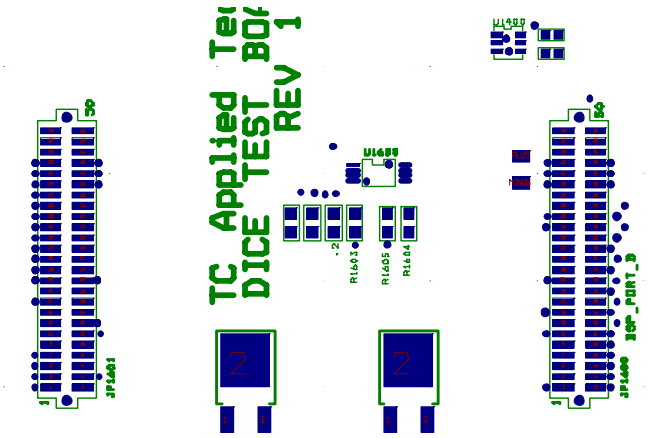


Figure 27: DSP module connectors

PIN	Signal	Type
1	Ground	
2	DSP_NRST	I
3	Ground	
4	Ground	
5	Ground	
6	DSP_IRQ	I
7	Ground	
8	DSP_EMPT	I
9	TP1607	
10	DSP_F1	I/O
11	TP1606	
12	DSP_CLKO	O
13	TP1605	
14	Ground	
15	TP1604	
16	DSP_A22	O
17	Ground	
18	DSP_NWR	O
19	DSP_CLK	
20	DSP_NRD	O
21	Ground	
22	Ground	
23	Ground	
24	DSP_D7	I/O
25	Ground	
26	DSP_D6	I/O
27	Ground	
28	DSP_D5	I/O

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29	Ground	
30	DSP_D4	I/O
31	Ground	
32	DSP_D3	I/O
33	Ground	
34	DSP_D2	I/O
35	Ground	
36	DSP_D1	I/O
37	Ground	
38	DSP_D0	I/O
39	Ground	
40	Ground	
41	3.3V	
42	3.3V	
43	3.3V	
44	3.3V	
45	NIL	
46	NIL	
47	NIL	
48	NIL	
49	NIL	
50	NIL	

Table 23: DSP Port A - JP1601 pin assignment

PIN	Signal	Type
1	Ground	
2	Ground	
3	FLAG3 (SPI_CS)	
4	Ground	
5	FLAG2 (SPI_DOUT)	
6	Ground	
7	FLAG1 (SPI_DIN)	
8	Ground	
9	FLAG0 (SPI_CLK)	
10	Ground	
11	Ground	
12	Ground	
13	DSAI_CLK	I
14	DSP_DSAI_RX3	O
15	DSAI_SYNC	I
16	Ground	
17	DSAI_DT	O
18	DSP_DSAI_RX2	O
19	DSAI_DR	I
20	Ground	
21	Ground	
22	DSP_DSAI_TX3	I
23	DSP_MCK	I
24	Ground	
25	DSP_SCLK	I

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26	DSP_DSAI_TX2	I
27	DSP_LRCK	I
28	Ground	
29	DSP_DT	O
30	TP1603	
31	DSP_DR	I
32	TP1602	
33	Ground	
34	TP1601	
35	I2C_CLK	I/O
36	TP1600	
37	I2C_DATA	I/O
38	Ground	
39	Ground	
40	Ground	
41	3.3V	
42	3.3V	
43	3.3V	
44	3.3V	
45	NIL	
46	NIL	
47	NIL	
48	NIL	
49	NIL	
50	NIL	

Table 24: DSP Port B - JP1600 pin assignment

50 position connector		
Manufacturer	**Mother Board**	**DICE Module**
SAMTEC	SFM-125-02-S-D-LC	TFM-125-12-S-D-LC

Table 25: DSP Port Connector Types

For connector JP1600 and JP1601 mechanical pin assignments, please see the previous section for same connector type.

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7 CPLD Configuration

7.1 Configuration

The U1200, Altera CPLD EPM240-T100, is the main device used to interface with user provided hardware. All signals required for parallel data communication with the DICE embedded ARM processor, such as data D0 through D15, address A0 through A3, byte-select BS0 and BS1, chip select NCS2 and NCS3, control signals NRD, NWR and NRST, are connected to this CPLD.

For user interface, 8 LEDs (D1216 through D1223) and an 8 bit preset DIP switch (SW1200) is provided. See section 3.4. SW1200 switches are connected to the CPLD and internally register mapped for convenience.

Two data ports, JP1201 and JP1202, are also connected to the CPLD with total of 15 data lines and a master reset signal. All data lines can be reconfigured to suit the user's needs through the CPLD's JTAG port JP1203.

NC2	A[0..2]	BIT	Description	Default value	Access Mode
0	000		**Control register**		R/W
		7	DICE parallel bus access enable. 0:Disable, 1:Enable	0	
		6	CODEC Enable. 0:Disable, 1:Enable	1	
		5	SPI Port-1 select. 0:Disable, 1:Enable	1	
		4	SPI Port-0 select. -//-	1	
		3	LED & DIP switch mode. 0:POST, 1:User	0	
		2	UIB_D port bit 7~4 mode. 0:Output, 1:Input	0	
		1	UIB_D port bit 3~0 mode. 0:Output, 1:Input	0	
		0	UIB_D port mode. 0:POST, 1:User	0	
0	001		**Status Register**		R
		7~1	Reserved	0	
		0	SPI port busy status	0	
0	010		**UIB_D port data**		R/W
		7~0	UIB_D port data	0	
0	011		**LED data**		R/W
		7~0	LED data	0	
0	100		**DIP switch data**		R
		3~0	DIP switch bit 0~3 data	0	
0		7~4	Reserved		
0	101	7~0	**Reserved**	0x00	-
0	110	7~0	**Reserved**	0x00	-
0	111	7~0	**Firmware version**	0x11	R
1	XXX		**Invalid**		

Table 26: User_IO interface CPLD - U1200 register map

In the default setup, UIA port D1~D3 act as Read, Write and Select signals. 256Fs, 64Fs and Fs signals are output on UIC port D0 ~ D2.

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8 Summary

The DICE EVM 002 provides a flexible evaluation and development platform for the DICE II, DICE Jr and DICE Mini chip family. The EVM is part of a complete and easy to use solution for development of advanced, high-performance audio devices, including Firmware, Host computer Drivers, Utilities and User Interfaces. Contact TCAT for EVM and Microboard design files, chip User Guides, Firmware development kit, Host development kits and other software.

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